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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,817	07/14/2003	Toshio Teraishi	03DCOAI1030	5232

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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,817	TERAISHI, TOSHIO	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4-11 and 16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 3-11 and 16-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 09/22/2006.

Drawings

2. The drawings are objected to because the test input terminal is not connected with the shift register in Fig. 1 as claimed. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On Page 8, Line 22 should recite single instead of sibgle. Appropriate correction is required.

Claim Objections

4. Claim 15 objected to because of the following informalities: It seems that claim 15 depends from claim 12 not claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Imamura (US Pat. 5,225,774)*** in view of ***Tsujii et al. (US Pat. 6,519,728)***.

Regarding claim 1, ***Imamura*** shows (Figures 1-6) a semiconductor integrated circuit comprising: a single test signal input terminal [214]; a single test signal output terminal [218]; a shift register [206] having an input terminal, which is connected to the test signal input terminal, output bits of the shift register being equal to a number of the output terminals of the LSI chip [201], and a voltage level of one of the output bits of the shift register being different from these of other output bits; and a plurality of switches [244, 245, 246, 247, 248, 249, 250],

each of which includes an input terminal, an output terminal and a control terminal (coming from [251]), a number of the switches being equal to the number of the output terminals of the LSI chip, each input terminal of the switches being connected to one of the output terminals of the LSI chip, the output terminals of the switches being commonly connected to the test signal output terminal, and each control terminal of each switch being connected to one of the output bits of the shift register.

Imamura fails to disclose the shift register in response to a clock pulse, further including a clock input terminal, the clock input signal is inputted to the clock input terminal from an external device. However, ***Tsujii et al.*** shows (Figures 2-5) a LSI chip responsive to a clock pulse, further including a clock input terminal, the clock input signal is inputted to the clock input terminal from an external device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Tsujii et al.*** into the device of ***Imamura*** by providing a clock input terminal to provide a clock pulse. The ordinary artisan would have been motivated to modify ***Imamura*** in the manner set forth above for the purpose of sending test signals at different time intervals to be able to send a plurality of test signals to test the LSI chip.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Imamura (US Pat. 5,225,774)*** and ***Tsujii et al. (US Pat. 6,519,728)*** as applied to claim 1 above, and further in view of ***Sakaguchi et al. (US Pat 6,850,085)***.

Regarding claim 2, the combination of ***Imamura*** and ***Tsujii et al.*** discloses everything as claimed above in claim 1.

The combination of ***Imamura*** and ***Tsujii et al.*** fails to disclose wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal. However, ***Sakaguchi et al.*** discloses (Col 15, Ln 35-44) wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Sakaguchi et al.*** into the device of the combination of ***Imamura*** and ***Tsujii et al.*** by providing an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal. The ordinary artisan would have been motivated to modify the combination of ***Imamura*** and ***Tsujii et al.*** in the manner set forth above for the purpose of reducing the cost of the LSI tester since it won't need digital circuitry.

8. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Tsujii et al. (US Pat. 6,519,728)*** in view of ***Imamura (US Pat. 5,225,774)***.

Regarding claim 12, ***Tsujii et al.*** shows (Figures 1-5) a semiconductor integrated circuit having test circuit comprising: a plurality of input leads [11, 12, 13, 16, 17, 18], each of which is formed in the user area and extended in a first direction to the non-user area; a plurality of output leads [14, 19], each of which is formed in the user area and extended in a second direction, which is different from the first direction, to the non-user area.

Tsujii et al. fails to disclose a single test signal input lead, which is formed in the user area and extended in the first direction to the non-user area; and a single test signal output lead, which is formed in the user area and extended in the first direction to the non-user area. However, ***Imamura*** shows (Figures 1-6) a single test signal input lead [214], which is formed in the user area and extended in the first direction to the non-user area; and a single test signal output lead [218], which is formed in the user area and extended in the first direction to the non-user area.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Imamura*** into the device of ***Tsujii et al.*** by replacing the LSI chip of ***Tsujii et al.*** with the LSI chip of ***Imamura***. The ordinary artisan would have been motivated to modify ***Tsujii et al.*** in the manner set forth above for the purpose of having a user and a non-user are in order to have an overall space to work without committing any testing errors.

Regarding claim 13, the combination of ***Tsujii et al.*** and ***Imamura*** discloses everything as claimed above in claim 12; in addition, ***Tsujii et al.*** shows (Figures 1-5) a plurality of test pads [3a-3d] formed in the non-user area, each of which is connected to one of the output leads.

Regarding claim 14, the combination of ***Tsujii et al.*** and ***Imamura*** discloses everything as claimed above in claim 12; in addition, ***Tsujii et al.*** shows (Figures 1-5) wherein a width of the test signal output lead is wider than that of each output lead.

Regarding claim 15, the combination of ***Tsujii et al.*** and ***Imamura*** discloses everything as claimed above in claim 12; in addition, ***Tsujii et al.*** shows (Figures 1-5) wherein the test signal input lead and the test signal output lead sandwich the input leads.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sato et al. (US Pat. 4,912,395) shows (Figures 1-4) a testable LSI Device incorporating latch/shift registers and method of testing the same.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Roberto Velez
Patent Examiner

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PRIMARY EXAMINER
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12/11/06